Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Please cancel claims 2 and 10-17.

1 (Currently amended): A semiconductor device comprising:

a first dielectric layer formed on a substrate;

a second dielectric layer formed on the first dielectric layer;

a stud formed through the first and second dielectric layers;

a third dielectric layer formed over a top of the stud; and

a first pad of first etch stop material formed ~~over the top surface of the stud and under the third dielectric layer~~ in an undermined region below the third dielectric layer remaining after removal of a portion of the second dielectric layer.

2 (Canceled)

3 (Original): The semiconductor device of claim 1 further comprising:

a first circuit region formed in the first dielectric layer, the first circuit region including the stud; and

a second circuit region formed in the first dielectric layer, the second circuit region including at least one conductive line and at least one spacer on a sidewall of the conductive line, the spacer being made of the same material as the first pad of the first etch stop material.

4 (Original): The semiconductor device of claim 1 wherein the third dielectric layer and the first etch stop material are the same material.

5 (Original): The semiconductor device of claim 1 further comprising a second pad of a second etch stop material formed over the top surface of the stud and the first pad of the first etch stop material, the second pad of the second etch stop material being selectively patterned to cover only an area of the semiconductor device that includes the stud.

6 (Original): The semiconductor device of claim 5 wherein the third dielectric layer, and the first and second etch stop materials are the same material.

7 (Original): The semiconductor device of claim 1 further comprising:

a first circuit region formed in the first dielectric layer, the first circuit region including the stud; and

a second circuit region formed in the first dielectric layer, the second circuit region including at least one conductive line and at least one spacer on a sidewall of the conductive line, the spacer being made of the same material as the first pad of the first etch stop material, whereby the spacers and the first pad are formed simultaneously.

8 (Original): The semiconductor device of claim 1 wherein the third dielectric layer has an etch selectivity with respect to the second dielectric layer.

9 (Original): The semiconductor device of claim 1 wherein the third dielectric layer comprises etch stop material.

10 (Canceled)

11 (Canceled)

12 (Canceled)

13 (Canceled)

14 (Canceled)

15 (Canceled)

16 (Canceled)

17 (Canceled)